REMARKS

Claims 1-20 remain for reconsideration. Claim 16 has been amended to correct a grammatical issue by adding the word "and" before the last recitation and not in light of any prior art rejection. No new matter has been added.

Applicants note with appreciation the Examiner indication that claims 7-20 are allowed over the prior art of record and further that claims 3-5 would be allowed if rewritten into independent form.

The sole rejection present in the application stands against claims 1, 2, and 6 under 35 U.S.C. § 102(e) as being anticipated by U.S. Published Application 2005/0053103 to Lo et al. (hereinafter "Lo"). This rejection is respectfully traversed based on the following discussion.

As noted by the Examiner, Lo contains common inventors with the present application and, in addition, is commonly assigned to Intel Corporation. However the Lo application was filed approximately 3 months prior to the present application therefore prompting the Examiner's rejection under 102(e).

In making the rejection, at least with regard to independent claim 1, the

Examiner is of the position that Lo identically discloses that which is recited in claim 1. In particular, the Examiner states that Lo teaches a first and second tunable elements and first and second error signals as well as the claimed "controller to linear relate said first error signal and said second error signal to output a first control signal to control said first tunable element and a second control signal to control said second tunable element" (emphasis added). For this teaching, the Examiner relies on Figure 4 and paragraphs 0034-0035 and 0038-0039.

However, Lo, including the relied upon passages,do not explicitly teach a "controller to linear relate said first error signal and said second error signal to output a first control signal to control said first tunable element and a second control signal to control said second tunable element" as claimed. In fact, Lo is silent on the point of linear relating a first and second error signal. That is not to say that its not possible for Lo to do so, it is simply not taught in the Lo application as required under 102(e).

MPEP § 2131 mandates that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT IN THE CLAIM". Furthermore, the MPEP, citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1051, 1053 (Fed. Cir. 1987), states "[t]he identical invention must be shown in as complete detail as is contained in the... claim" (emphasis added).

Here, Lo does not teach the recited "controller to linear relate said first error signal and said second error signal". It is therefore respectfully submitted that the rejections to the claims are improper under Section 102 as Lo cannot anticipate the rejected claims since they do not "teach the identical invention". Based on the above discussion with reference to the MPEP guidelines, it is respectfully requested that the rejections based on 35 U.S.C. § 102 be withdrawn.

This being the only rejection to claims 1, 2, and 6 it is respectfully requested that these claims be allowed.

In view of the foregoing, it requested that the application be reconsidered, that claims 1, 2, and 6 be allowed along with all other claims 1, 3-5, and 7-20 and that the application be passed to issue. Please charge any shortages and credit any overcharges to Intel's Deposit Account number 50-0221.

Respectfully submitted,

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